T5830ES System Introduction

Future Powerful & economical flash-WT/FT solution

Rev 1.2

CONFIDENTIAL
PRELIMINARY

T5830
Product Overview

ADVANTEST

T5830 Value Proposition

■ Fully Optimized, Scalable & Economical Flash Solution

✓ *T5800 series (AS-platform) module architecture to enhance ROI with less risk*

■ Full Functionality & Flexibility for Flash Test

- ✓ *Provides full WT & FT test coverage for LPC-SPI NOR/NAND and Smart cards*
- ✓ *All I/O architecture with plenty native VIHH resources for maximum flexibilty*
- ✓ *800Mbps sufficient performance in the segment*

■ Effective Resource Utilization

- ✓ *Test program compatibility: FutureSuite based*
- ✓ *Seamless platform transition from legacy install base*

■ Best CoT Performance

- ✓ *Enable Best COT performance*

Benchmark: Proved more than **20~50% TTR **& 30% CoT reduction** vs. legacy V-series Flash solution*

ADVANTEST

T5830ES Configuration

Target Applications

- NOR/NAND/(LPC SPI, FPC), embedded Flash as MCU, SRAM, other NVM

System Configuration

- **Speed**: 800Mbps
- **Max. PE channels**: 288full-IO (@1-TOM)
- **ES-MB**
- **(Optional) HV-level driver module**: 288 channel(@-10 to +30V: VSIM/MVM)

Parallelism(1-TOM)

- 72 DUT parallelism @ 4 digital pin (SPI-NOR/NAND)
- 48 DUT parallelism @ 6 digital pin (SPI-NOR/NAND)
- 18 DUT parallelism @ 16 digital pin (Typical NAND x8-DQ)

T5833ES System Specification

ITEM		T5830ES
Max. Frequency		400MHz/800Mbps
Accuracy	OTA	+/-350ps
	Dr/Cp Skew	200ps p-p
Site-CPU		2
ALPG		6
TH Channels	IO	288
	DR	-
	LVLDR	(Option HV-LVLDR -10 to +30v: 288)
	PPS	24(1.2A) x 2 port= 48(600mA)
VIHH		144 -> (1 per 2 I/O pins)
Passive Load		72 -> (1 per 4 I/O pins)
DC(PMU)		24
Formatter Channels		48IO

ADVANTEST

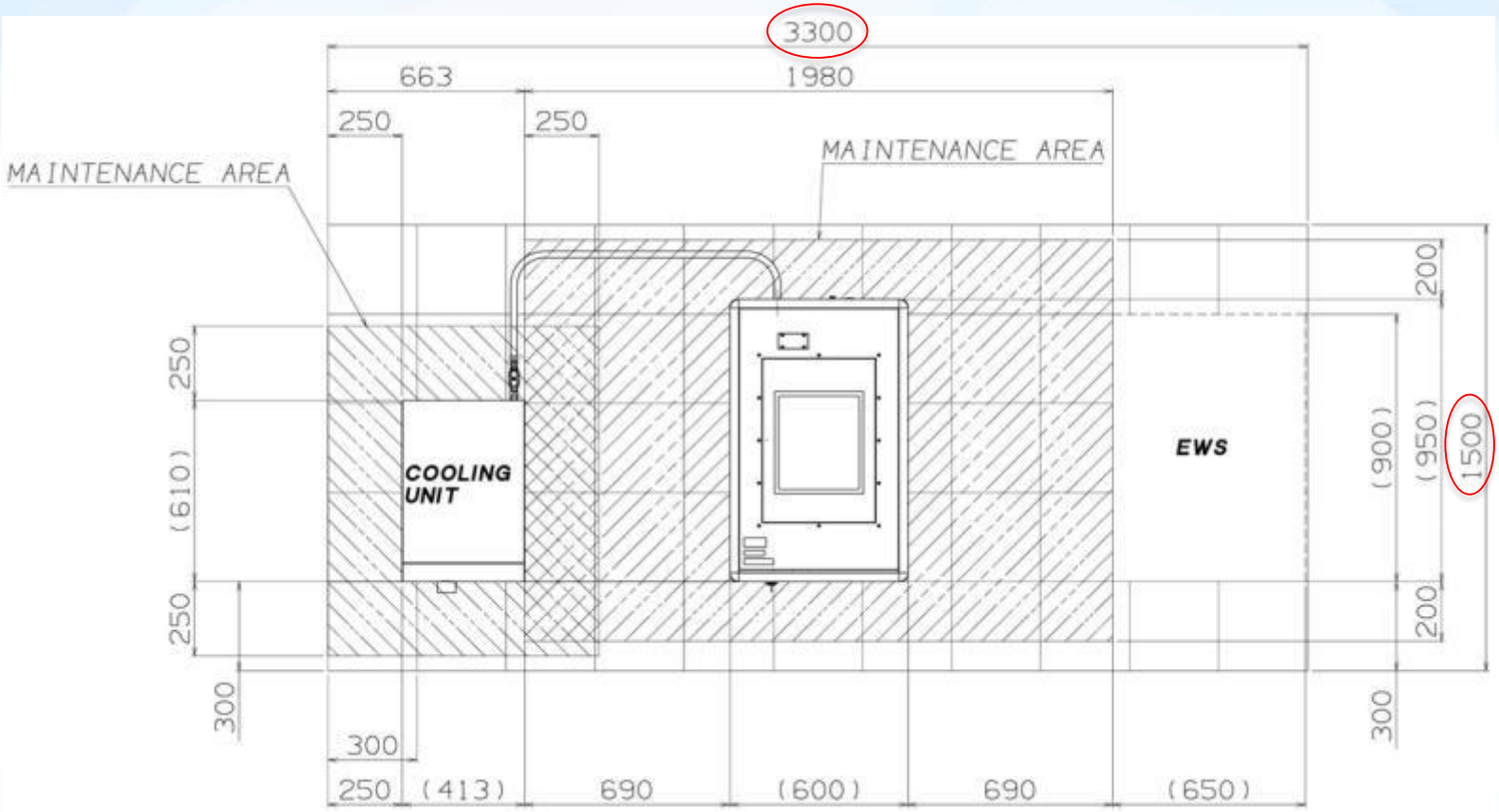
High Voltage Level Driver module (Optional)

High Voltage Level Driver Module (Optional)

ITEM		HV LVL DR
Channel		48 Units x 6 branch = 288 output ch/ module
VSIM	Output Voltage	−10V ～ +30V
	VS Resolution	4mV
	Current Measurement	−80mA ～ +90mA (per Unit)
	IM Resolution	40uA
	Max. Capacitive load	0.1 uF (per each 288 output ch)
MVM	Voltage Measurement	−10V ～ +30V
	VM Resolution	4mV

ADVANTEST

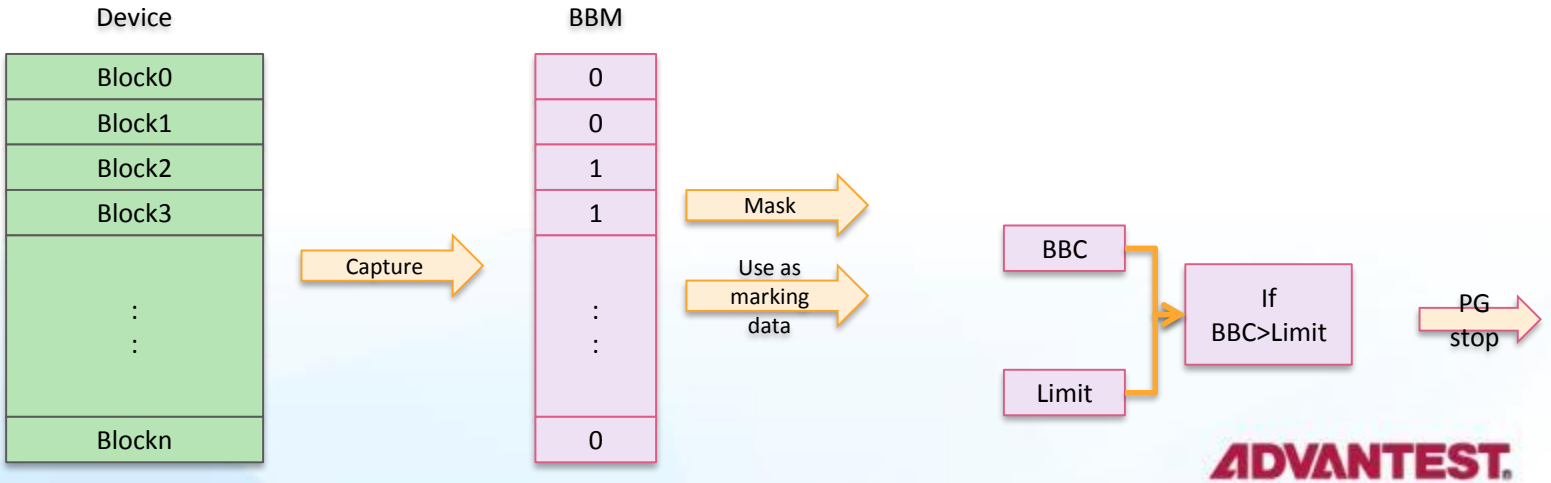
ES Floor Plan



T5830ES
Key Flash functions

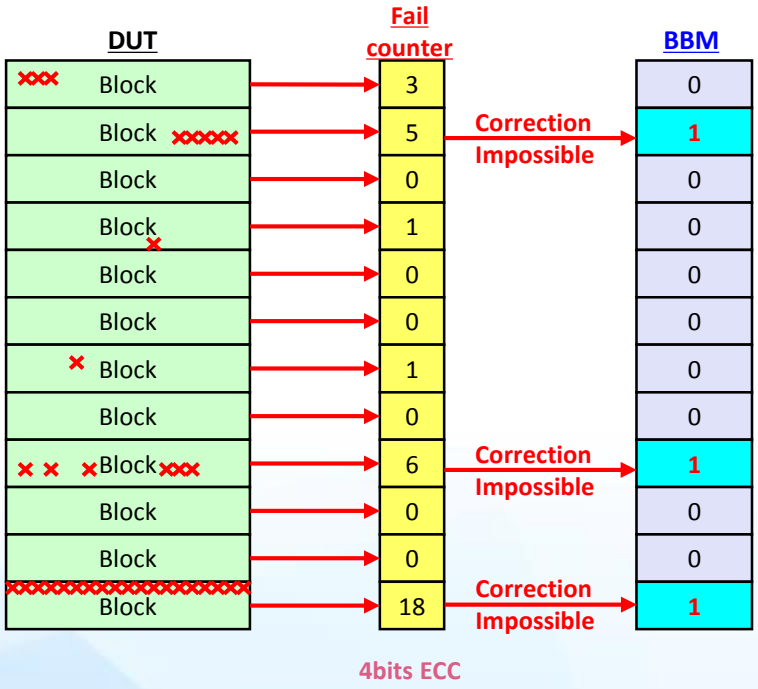
BBM-Bad Block Memory

- Purpose
  - One of fail capture memory.
  - Mainly manages failure of block.
- Use case in NAND testing
  - Easy to know where bad block Address is and the number of bad blocks.
  - If the target block is bad
    - Inhibit logical compare during the test
    - Inhibit program or erase operation
    - Easy bad block marking using this information
    - Stop pattern running if # of bad block exceed the limit.



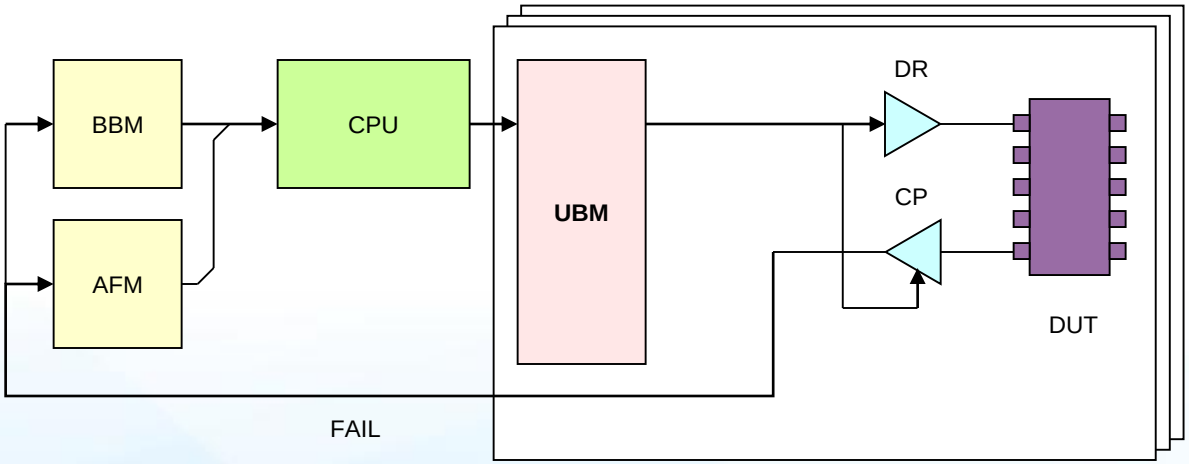
Real time fail count for ECC

- Purpose
  - Count number of failures in particular region and compare it with expected count during pattern running.
- Use case in NAND testing
  - Easy to know failure in region can be corrected by ECC or not.



UBM – Universal Buffer Memory

- Purpose
  - Generate DR or CP(expected) pattern for each DUT.
- Use case in NAND testing
  - Write/Read unique data into each devices at the same time
    - Unique Data : ID or bad block marking



ADVANTEST

PDS Memory (Serializer)

- Purpose
  - Easy to generate serial data from ALPG data (X/Y/data/command)
- Use case in NAND testing
  - Generate serial data for SPI device