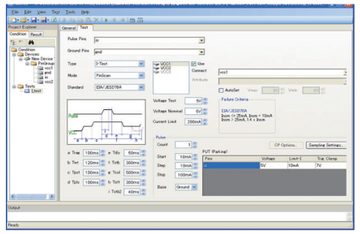
Latch-up test and measurement result

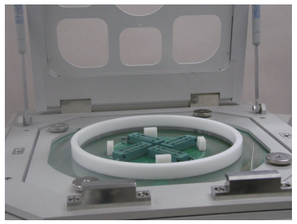
Setting of Latch-up test



The setting for the timing of inserting pulse or the time width with confirming the visual figure is possible.

Latch-up test meets EIA/JESD 78 specifications. Pass/Fail criteria can be specified by JEDEC JESD78A or JEDEC JESD78 or Users. Voltage and current waveforms can be displayed in Latch-up test.

Socket Board and Zap unit

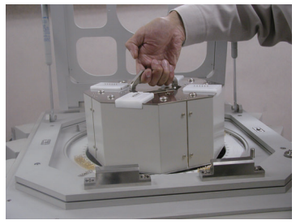


Socket board

Max. 8 sockets can be installed, and simultaneous zapping to each socket (these needs to discuss) is possible. Simultaneous zapping makes test time shorter.

Making of socket board that adaptable to every package is possible.

such as BGA Packaging Test Board Within 500 pins.
Or SOP Packaging type Test Board or 512 pins universal test board, in order to facilitate users to make adapter board.



Zap unit

Zap unit can be put and removed easily with desorption method.

Machine Model (MM)×2 and Human Body Model (HBM)×2 are featured as standard. Making zap unit as your option request is possible.

Multi-site HBM and MM parallel testing.

HANWA

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■ Agency

HCA_E_HED-N5000_20190613_*

Pin expansion to 1024
Automatic ESD Test System

HED-N5000 series

JEDEC, ESDA, AEC, JEITA
※include JS-001 and EIA/JESD78

HANWA Hanwa Electronic Ind. Co., Ltd.

Features

Low parastic ESD Tester available

Simultaneous plural zapping is practicable

Installing Max. 8 sockets and simultaneous plural zapping into each socket are possible.

Effective use of existing asset

Socket board, which is equipped with conventional, ESD test instrument is usable. (HED-S5000 series, HED-F5000series)

Adaptable to various standard waveforms

This corresponds with domestic and abroad standard such as JEITA, JEDEC and ESDA standards. ※include JS-001 and EIA/JESD78

Adaptable to Latch-up test

This corresponds with ESD pulse zapping method, V_{supply} over-voltage zapping method and constant current pulse zapping method.

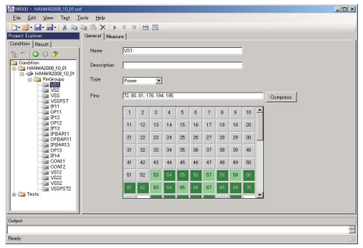
Vector (Option)

High performance relay with full electronic time control switching mode

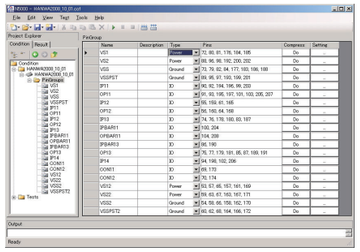
Setting of ESD test and measurement result

Windows OS, HBM/MM/Latch-up can be automatically switched by software, with discharge mode. It can realize automatic test combination between pins, automatic connection, automatic ESD test, Latch-up test and I/V characteristic test by programming. Document output can be compatible with the software format of most analysis software in the market.

Pin group setting

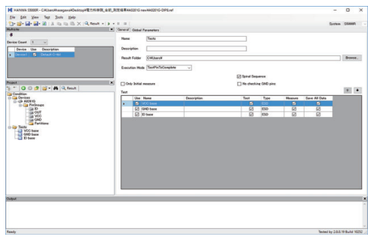


Measurement conditions of Leakage

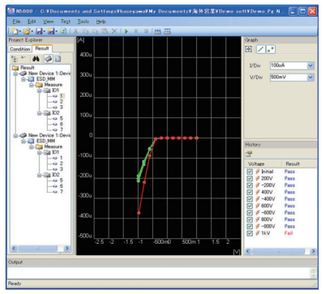


Automatically generate test data report, including test setting conditions, failure judgment conditions before and after test of all pins, results and detailed I/V characteristic scanning curve. I/V leakage measurement of different pins can automatically complete and save data, and the data format can be read and arranged in Excel format.

Test plan setting



ESD Result



The configuration and function of system

The equipment provides you the choice of test pin number:256 pins, 512 pins, 768 pins and 1024 pins.
※ 2 ～ 6 signifies DC power supply for bias. 2 represents 2 power supply type, 6 represents 6 power supply.

Model	Test pin	ESD Test	Latch-up test (Option)
HED-N5256-D2/6	256pin	<Support for standards> Corresponds with JEITA , JEDEC, ESDA and AEC <Test model> MM(200PF, 0Ω)×2 HBM(100PF,1500Ω)×2 are featured as standard.	<Support for standards> Corresponds with JEITA , JEDEC and AEC <Test model> ESD Latch-up test (200PF, 0Ω) Constant current Latch-up test V_{supply} over-voltage test
HED-N5512-D2/6	512pin		
HED-N5768-D2/6	768pin		
HED-N51024-D2/6	1024pin		

Specification

Equipment model	HED-N5000
Capacity of power supply	256 and 512 pins - 100VA, 768 and 1024 pins - 200VA
Pin number of max. measurement	256 pins, 512 pins, 768 pins and 1024 pins
Pulse zapping unit	MM×2 and HBM×2 are featured as standard
Pulse voltage	MM:10 ～ ±4000V, HBM:10 ～ ±8000V (Option)
Pulse voltage step	±5V
Pulse zapping number	1 ～ 99 times
Pulse interval	0.1 ～ 9.9s
Voltage polarity	+, −, +/−, −/+
Accuracy of charge voltage	1% x ESD charge voltage ±10V
Bias DC power supply	±35V/1A (Option: ±100V/1A, 30V/5A)
Supply voltage accuracy for Latch-up measurement	1%±50mV
Supply voltage step	0.1V
Current pulse width	0.1 ～ 100ms
Clamp voltage (I-test)	1 ～ 100V
Clamp voltage step (I-test)	0.1V
Vsupply over-voltage power (for Latch-up test)	100V(1V step)
Vf/Im measurement power supply IV Curve scanning with full 512 Channels or higher	±40V (0.1V step) / 100 mA (Option：±100V/±1A)
Accuracy of Vf/Im measurement	1%±（1/500FS±10n A）
Vf/Im measurement point	100 point
Pulse current supply	±1A（1mA step)
Max count power supply	8
Wave form sampling (for Latch-up test)	10MHz, Max.4000 points
Destruction judgement	Changing amount judgement / Absolute value judgement
Vector (Option)	
Outer dimensions	1600mm(W)×900mm(D)×1500mm(H)
Weight	150 Kg ～ 200 Kg
Basic software(OS)	Windows