Anadyne
Precision Analog Design

Rev 1.1

Spec sheet for:

L17D#A
L17D#B
L2010v3 die

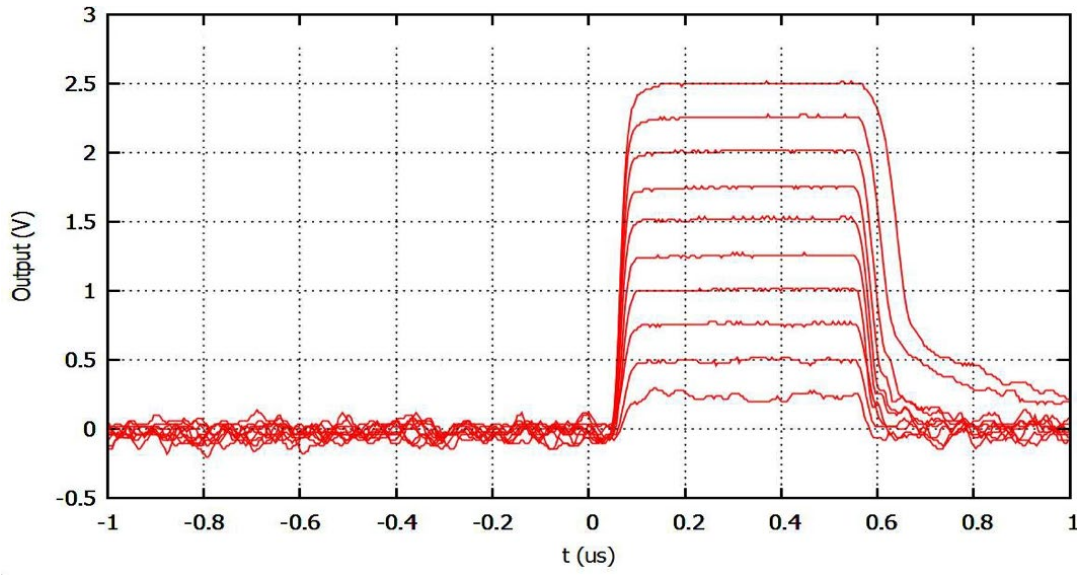
This spec sheet is a truncated version of our more detailed application notes, which can be found on our website: www.anadyneinc.com.

General Description:

- ANADYNE's Fast Ultra Low Noise Preamp; Compatible with many different input topologies for maximum flexibility.
- Two More Linear Amplifiers; Integrated amplifiers allow for very low propagation delay and high dynamic range.
- Eleven Log and Linear Extension Stages; Many of the stages are tunable making very precise and custom non linear transfers possible.
- Direct Summing Junction for Dual LVA Circuits; Two or more L-17D's can be used in combination for even more dynamic range.
- Output Amplifier Stage; Our output amplifier can drive 50 ohm cables and now comes with a short circuit protection option.
- Packaged parts are hermetically sealed and thoroughly screened for high reliability applications.

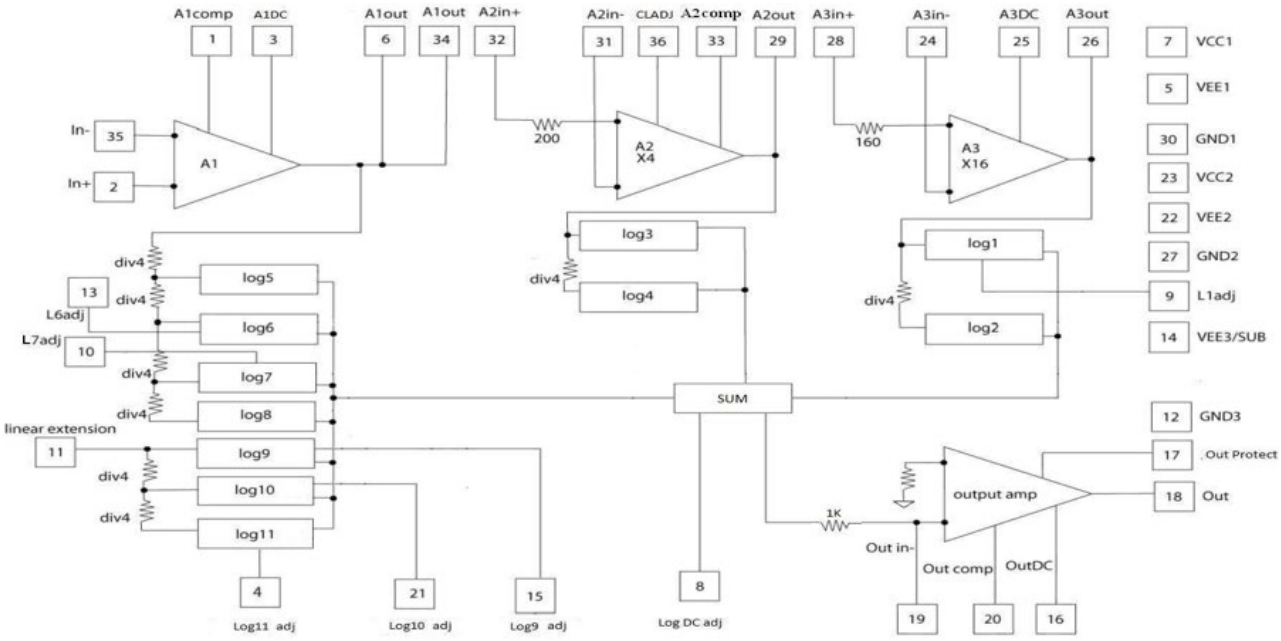
The L-17D transfer function is based on a piecewise linear approximation technique. For a more involved discussion of the theory of operation, please see the article “Theory of Operation of Logarithmic Amplifiers” article on the Anadyne, Inc. website.

Typical output using a biased schottky detector:



Notes: Pulse ladder has 5 dBm increments between rungs.

L-17D Block Diagram:



Note: for pinout A: Out Protect and Out are internally connected

Specifications:

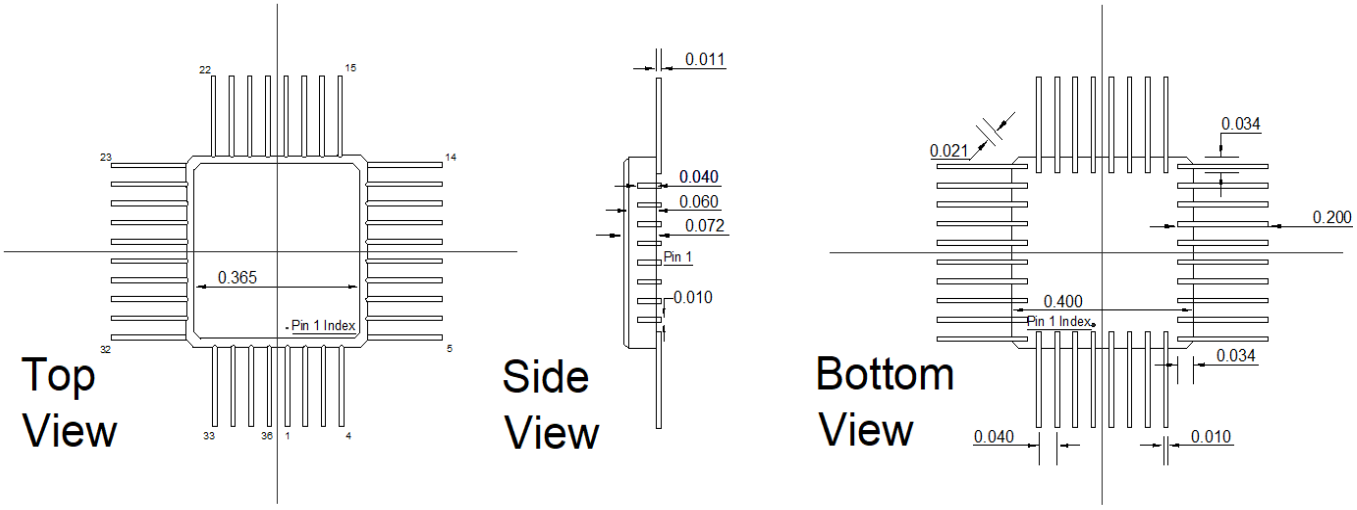
Parameter	Value	Notes
Package Size	10mm x 10mm packaged, 2x3 mm die	
Input Rail Voltages	+/-5V to +/- 7V	
Operating Temperature range	-55C to 95C	The L-17D is burned in under power at 150C
Current draws at +/-6V	32ma, I-, I+	
Dynamic range linear input	>92dBV positive input, 80dBV negative input	
Max dynamic range with tunnel diode	50dBm	
Max dynamic range with Schottky detector	65dBm	
Log linearity	Tunable to +/-1/3 dB	
Temperature drift	<0.5 dB after adjustment	
Input voltage noise density	1.2nv/√Hz	
Input current noise density	<1pa/√Hz	
Risetime (10% to 90%)	8ns	With full dynamic range, faster with 2 log stages eliminated
Transit time (50% to 50%)	8ns	Variation in transit time over full dynamic range can be tuned to <2ns
Pulse to CW variation	<.0.2dB	A change in pulse duration from 10 ns to 1 ms (at high duty-cycle) does not affect pulse height for DC coupled designs. For pseudo AC coupled designs 90%+ duty cycles are possible.
Fall time to 50mv output	<50 ns (with recovery nets)	
Max output voltage	VCC-2.1V	
Output drive capability	80ma	
Output slope	adjustable	

Absolute Maximum Ratings:

Parameter	Limits
Storage temperature	-65°C to +150°C
Operating temperature	-55°C to +125°C
Junction temperature	Up to 150°C
Rail voltages	±12V
Soldering temperature (Pinout A and B)	350°C for 60 seconds
A1 output current (pin 5)	70 mA
A1 output current (pin 34)	20 mA
A2 output current	10 mA
A3 output current	10 mA
Output driver current	80 mA, unless short circuit protection is used

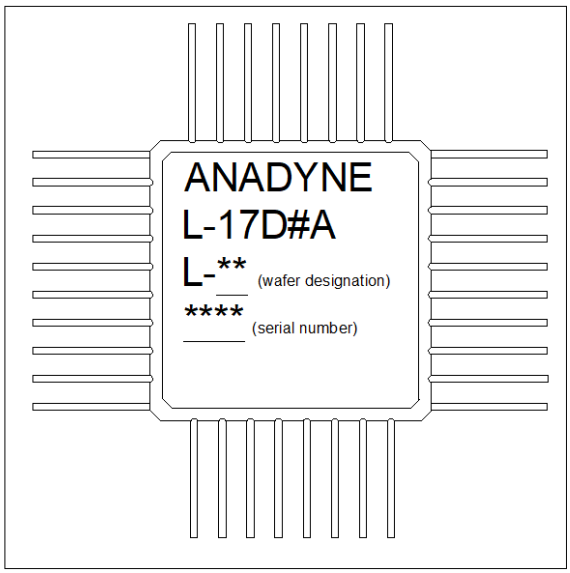
Package Dimensions:

For L-17D#A and L-17D#B parts.



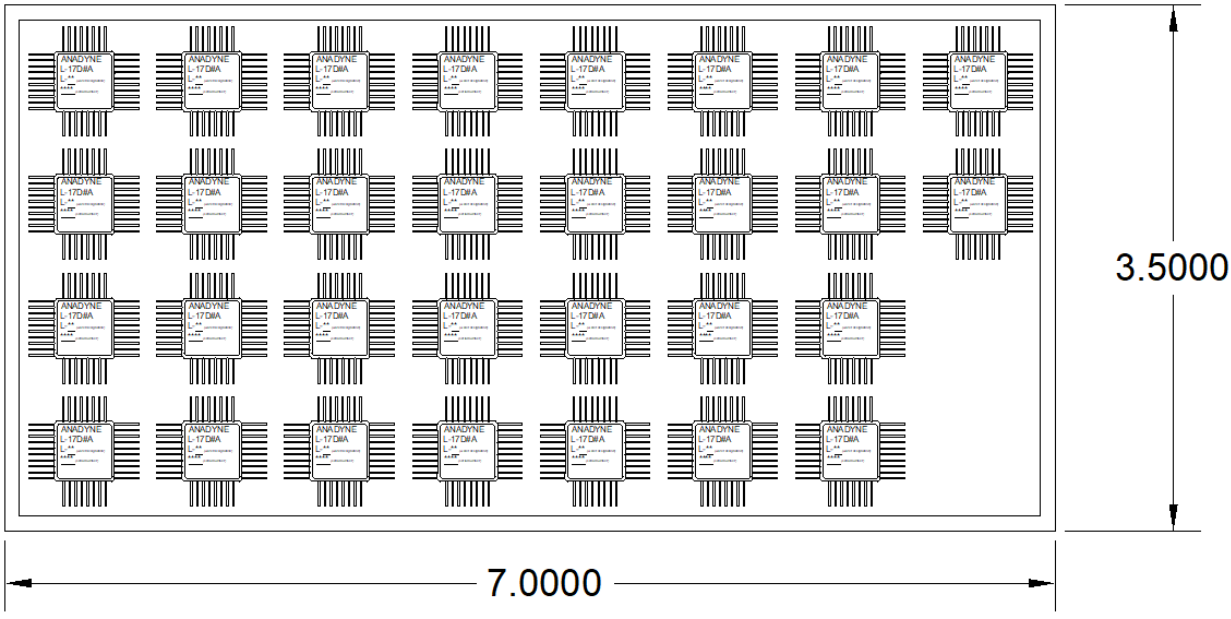
Notes: Typical values, shown in inches.

Part Labeling:



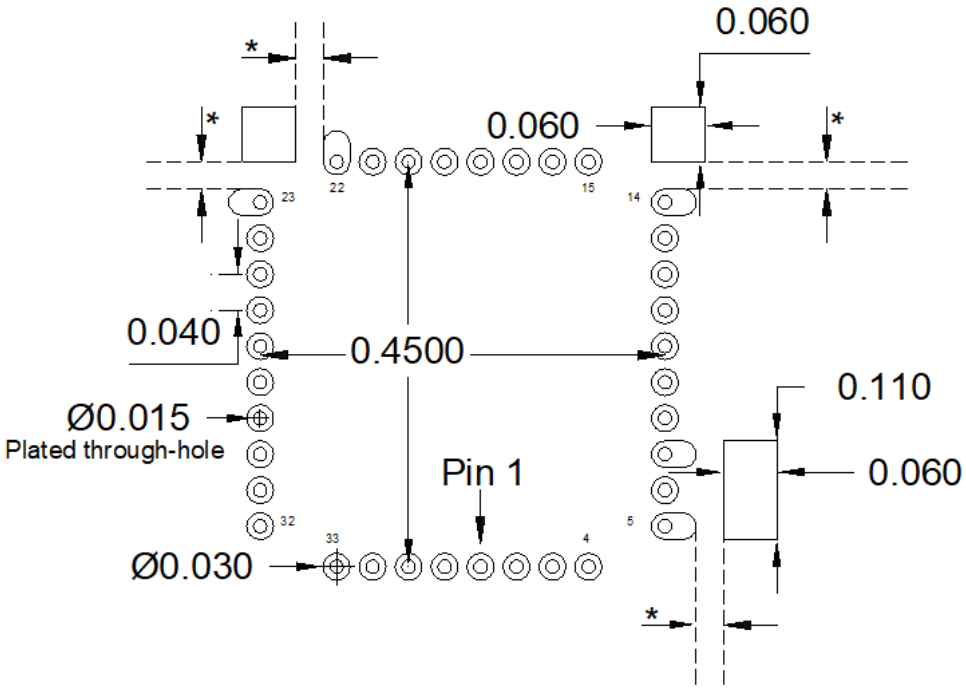
Notes: #A pinout shown in this example. This labelling convention effective November 2018.

Shipping Packaging:



Dimensions in inches. L-17D parts are shipped in conductive plastic packaging with soft conductive foam padding, with up to 30 parts per box in the following arrangement unless instructions are given and agreed upon ahead of time.

Sample PCB footprint:

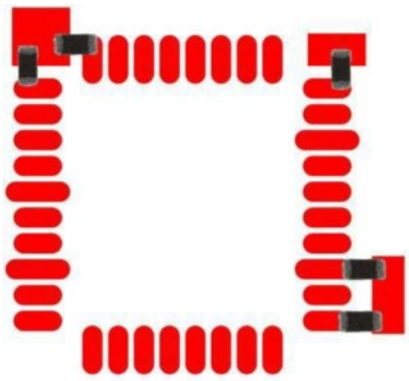


* Adjust metal ground pad to pin spacing to accomodate bypassing capacitor of choice.

Dimensions in inches.

Note: Customer's will often generate a jig to bend the L-17D legs to fit the holes in their footprint. Some customers use the L-17D packaged part as a surface mount component instead of feeding the pins through holes in the board with no adverse effects in high reliability applications.

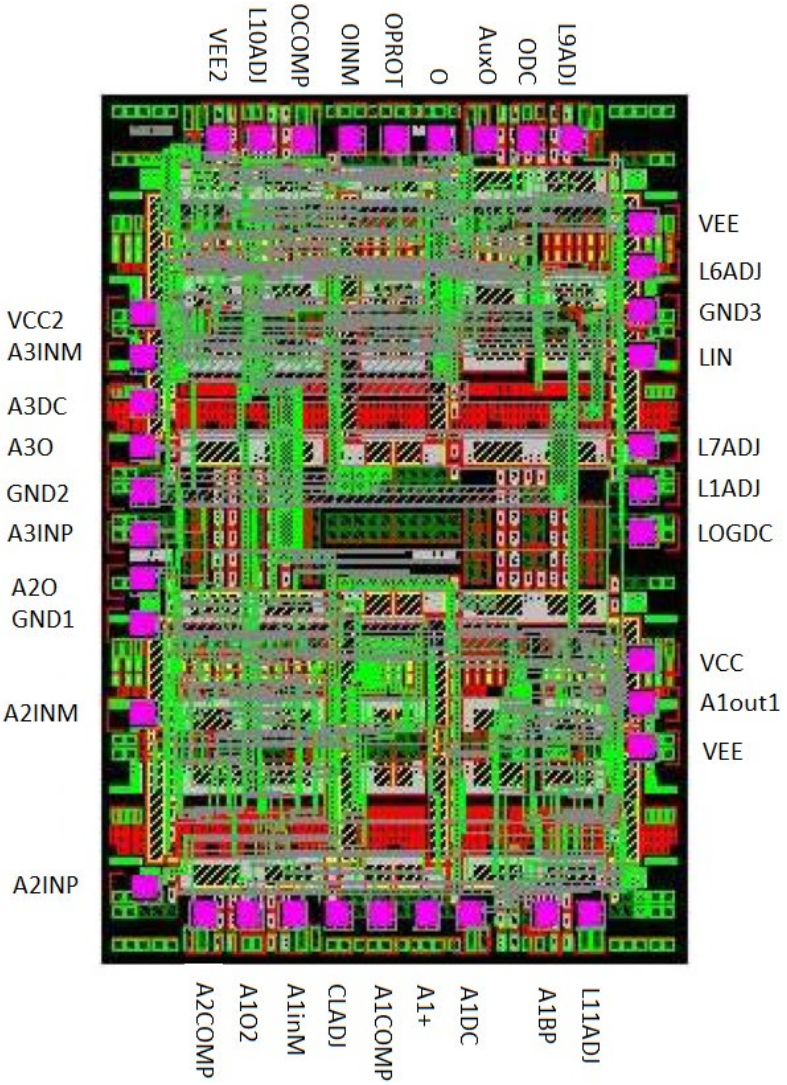
Sample bypassing diagram:



Die Pad Layout:

For the L2010v3 die.

Pad coordinates:	x (µm)	y (µm)
A2COMP	336	128
A1O2	496	128
A1INM	656	128
CLADJ	816	128
A1COMP	976	128
A1+	1136	128
A1DC	1296	128
A1BP	1564	128
L11ADJ	1724	128
VEE	1908	732
A1OUT1	1904	892
VCC	1904	1093
LOGDC	1904	1504
L1ADJ	1904	1664
L7ADJ	1904	1824
LIN	1904	2144
GND3	1904	2304
L6ADJ	1904	2464
VEE(SUB)	1904	2624
L9ADJ	1664	2920
ODC	1504	2920
AUXO	1344	2920
O	1184	2920
OPROT	1024	2920
OINM	864	2920
OCOMP	704	2920
L10ADJ	544	2920
VEE2	384	2920
VCC2	128	2292
A3INM	128	2132
A3DC	128	1972
A3O	128	1812
GND2	128	1652
A3INP	128	1492
A2O	128	1332
GND1	128	1172
A2INM	128	852
A2INP	128	224



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